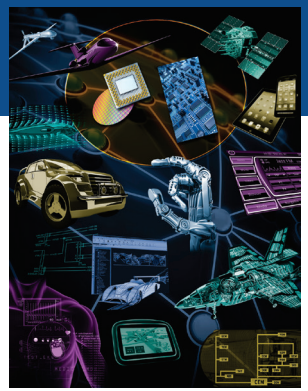
# Advanced Process Node Server Processor Design: Successful Implementation of Enhanced Calibre SmartFill Methodology

Mentor, a Siemens Business / Qualcomm

# ABSTRACT

The impact of fill on the various manufacturing processes has gone well beyond basic CMP. Fill rules are increasing in complexity, and compliance is becoming more difficult to achieve. This creates a significant pressure to find a fill methodology that meets foundry manufacturing requirements, while minimizing timing impact to the design, yet still maintain tape out schedules. To help achieve these disparate requirements, TSMC and Mentor worked together to develop a Calibre ECO Fill flow. Qualcomm used the ECO Fill flow co-developed with TSMC, based upon Calibre® YieldEnhancer SmartFill technology, to meet their time to market requirements. In this presentation Mentor and Qualcomm, will present the Quality of Results numbers from SmartFill ECO Fill flow in achieving DRC density, minimizing timing impact, and reducing the fill runtimes, for what is now POR at Qualcomm Server.

# Calibre® YieldEnhancer



## Advanced Process Node Server Processor Design: Successful Implementation of Enhanced Calibre SmartFill Methodology

John Waida
Sr. Staff Engineer Datacenter Technologies Inc.
Qualcomm

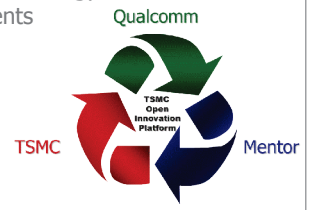
Jeff Wilson
Calibre DFM Marketing Director
Calibre Design Solutions

TSMC Open Innovation Platform 2017

Mentor A Siemens Business

## Introduction for Today's Presentation

- Complexity of fill requires a tight partnership
  - Customers benefit from a TSMC and Mentor Partnership
- Design community benefits from TSMC's Open Innovation Platform
  - TSMC specify the design rules based on process technology
  - Qualcomm Design teams build to these requirements
  - Calibre verifies that it is done correctly
- Mentor working with Qualcomm
  - Using existing products to augment the fill decks
  - Moving beyond fill by solving design flow issues

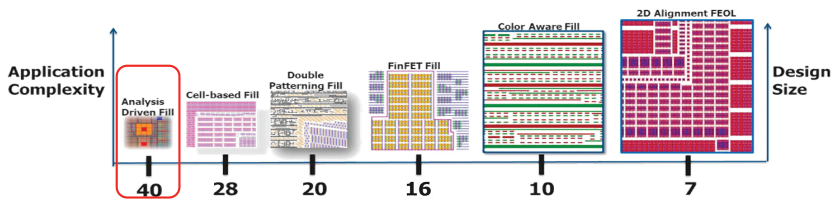







## TSMC and Mentor Working Together

- N40 and above: Analysis-Driven Fill is the basis for SmartFill
  - Original functionality requested by TSMC
    - ❑Maximum and gradient density control

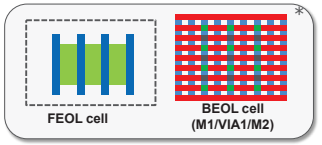


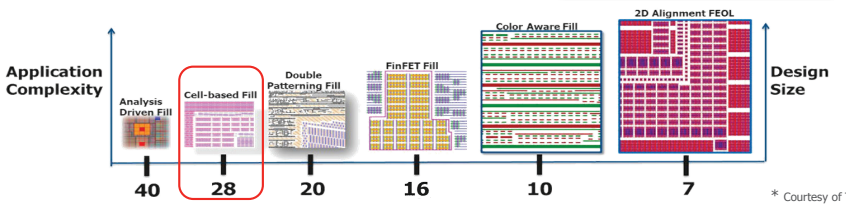





## TSMC and Mentor Working Together

- N28: Cell-based fill reduces runtime and file size
- Designed for multi-layer fill cells
  - FEOL options that look like transistors
  - BEOL options that add via stack

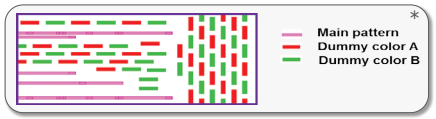


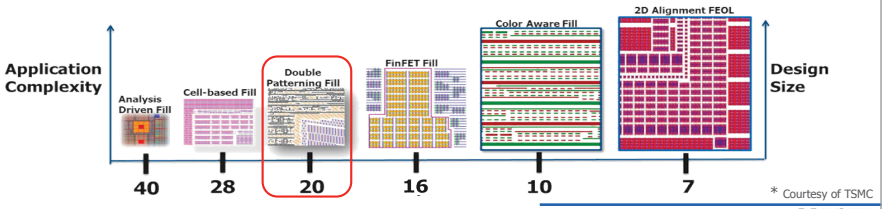




* Courtesy of TSMC

## TSMC and Mentor Working Together

- N20: Automatic double-patterning fill
  - — Evenly distributes two colors
  - — Expandable to support triple and quad patterning



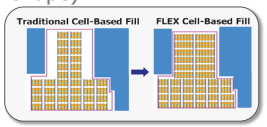

* Courtesy of TSMC

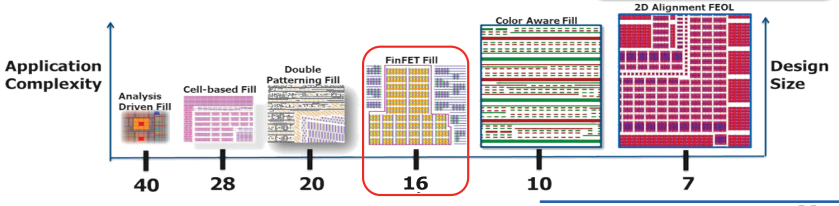




## TSMC and Mentor Working Together

- N16: Address FinFET constraint to keep all fill shapes aligned
  - — Leverage the existing cell-based approach (1D flex shape)
  - — Maximize insertion rate to meet uniformity target
  - — Insert FEOL cells to align with FinFET grids



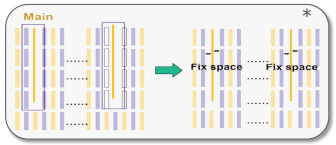



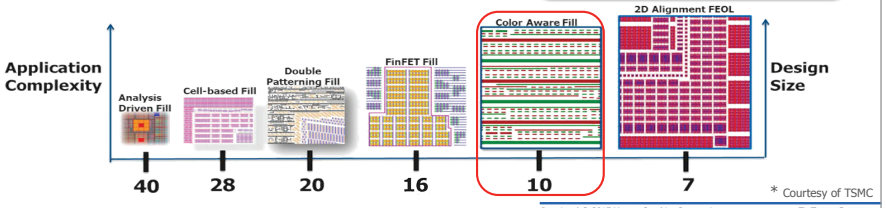





## TSMC and Mentor Working Together

- N10: Wrap interconnect with color and maximize insertion density
  - — Taking care of all the low-level details
    - ❑ Special alignment constraints
    - ❑ Voltage- and width-dependent spacing
  - — Further enhancement to maximize insertion



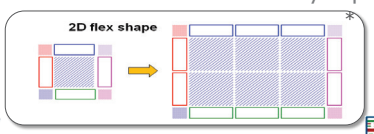

* Courtesy of TSMC

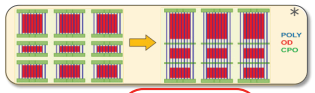


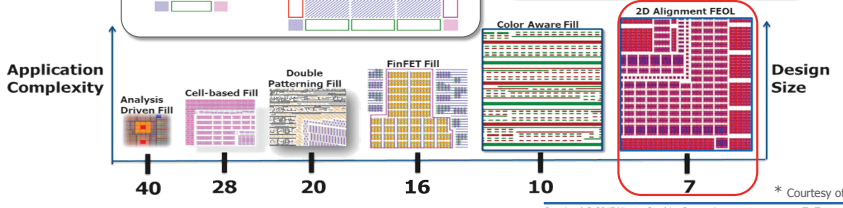


## TSMC and Mentor Working Together

- N7/N10: Extend 2D alignment in both directions by unit cells
  - — Expand the functionality to maximize insertion rate
  - — Connect fill cells for local uniformity improvement




* Courtesy of TSMC

## Finding a Solution When Additional Work is Required

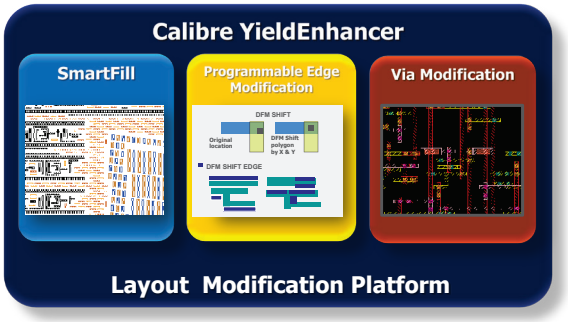
- Using existing technology to meet Qualcomm's design objectives
  - — Fill deck is designed to accomplish the vast majority of fill requirements
- At times a design choice requires additional work to achieve the required density
  - — Power Grid structure was already determined
  - — Given the size and spacing requirements one layer was missing density
- Choices were to do the following
  - — Change the Power Structure (late in the process and a non-starter)
  - — Waive the violations (not the safest approach)
  - — Augment the fill deck to automatically achieve DRC-clean results





## Partnering Produces a Win – Win

- Using existing technology to meet Qualcomm's design objectives








QUALCOMM

# Successful Implementation of FillPlus Methodology for Server Processor Design

John Waida
Sr. Staff Engineer
Mike Cesky
Sr. Engineer
Qualcomm Datacenter Technologies, Inc. (QDT)
September 13, 2017
#whywait

## Agenda

- Problem Statement : Meeting density physical design rules
- Solution : FillPlus supplemental fill methodology
- Details on how FillPlus achieves Density
  - — Examples
- Summary

## Qualcomm Datacenter Technologies, Inc. (QDT) Announcements / Press Releases

THE WALL STREET JOURNAL

### Qualcomm Unveils Chip to Attack Intel Server Stronghold

The Centriq 2400 processor, which is shipping in sample quantities to be tested by big web services, is expected to be available broadly in the second half of 2017

By DON CLARK
Dec. 7, 2016 7:30 a.m. ET

Qualcomm Centriq is a product of Qualcomm Datacenter Technologies, Inc.

## Problem Statement

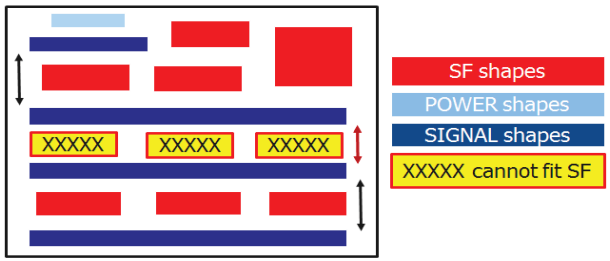
**Needed a metal fill methodology that**

- Achieves the density and physical design rules
  - Deck from factory does not meet density requirements on our design, as we utilized a unique BEOL power structure
- Minimized timing impact to the design
  - Need to minimize the amount of fill that is added next to signal lines
- Introduces zero new DRC violations
- Easily fit into an existing flow
- Minimized runtime impact to design flow
  - Important to keep as much fill as possible on the fill datatypes
    - Reduces Post Fill DRC and LVS run times

## Reasons Why Density Originally Was Not Achieved

- Rules for POR fill shapes insertion:
  - Spacing and size of fill shapes are larger than drawn shapes
  - Rules created conflicts especially around selected Power Structure, Clock Line and Pre-routes



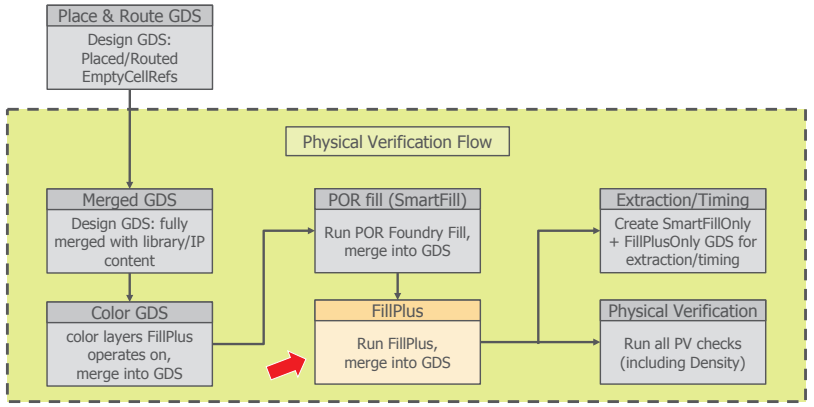

 

## FILLPlus Solution To Meeting Density Rules

- Development: collaboration of Mentor and QDT
- SVRF deck that runs after SmartFill POR fill deck
  - Run after the design is colored to take advantage of different color spacing
- Inserts additional shapes into the design
  - On 'design' layers (not 'fill' layers)
  - Able to insert in areas where fill shapes cannot fit
  - Extends existing (power) shapes
- Shapes inserted strategically to
  - Meet density specifications
  - Minimize timing impact
  - Be DRC-clean

## FillPlus : Implementation In The Flow



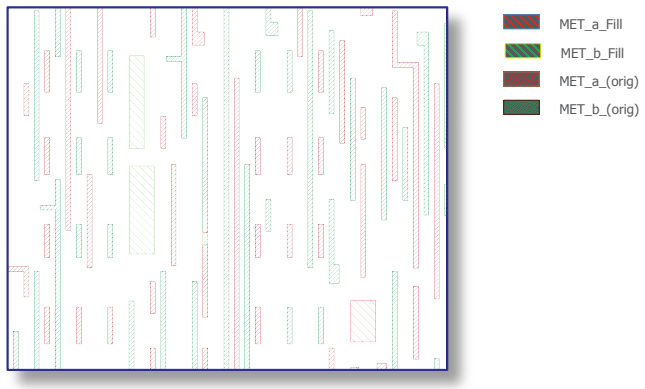
## What the FillPlus Solution Offered

- Integrated well into design flow
  - — Only used when required
- Simple add-on to flow:
  - — Runs right after POR SmartFill deck
- Design database size:
  - — Minimal increase : only density-failing regions have shapes inserted
- Fast run times
  - — Example: "medium size" blocks: FillPlus took 30 minutes
- Timing impact: minimal
  - — Comparable Timing Results of "SmartFill-only" versus "SmartFill + FillPlus"

## FillPlus Code: PEM Example On Colored Layers

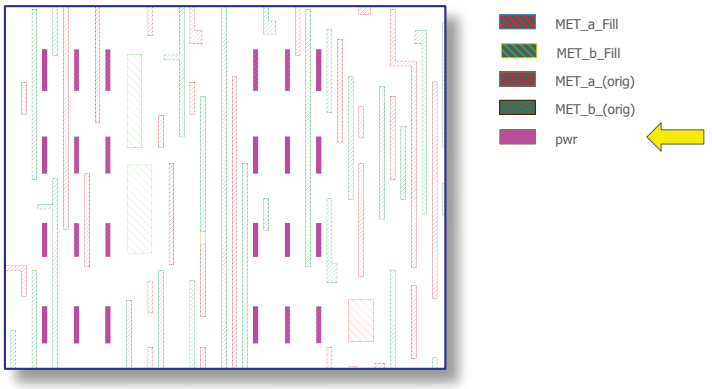
Colored metal layer after POR SmartFill (colored shapes)



## FillPlus Code: PEM Example On Colored Layers

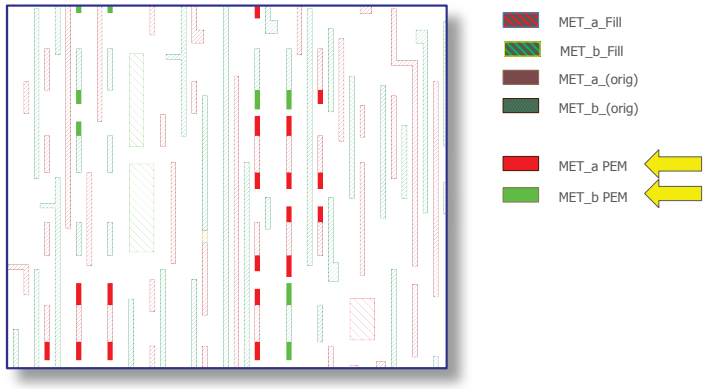
Identify certain power shapes for potential PEM NOTE: Lengthen only to avoid wide metal DRC's



## FillPlus Code: PEM Example On Colored Layers

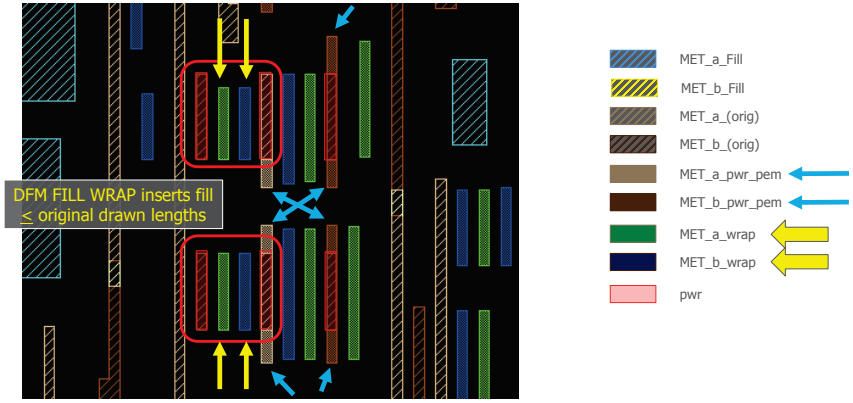
Extend key shapes detected, ensuring DRC compliant (including same/diff color DRC checks)







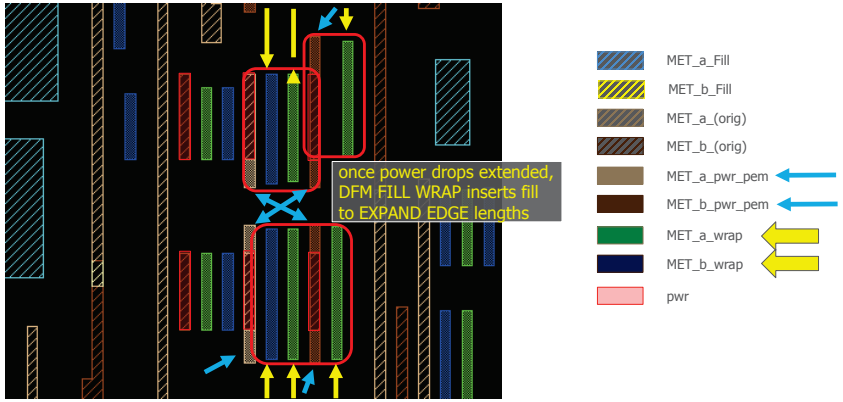
## FillPlus Code: Wrap Example On Colored Layers







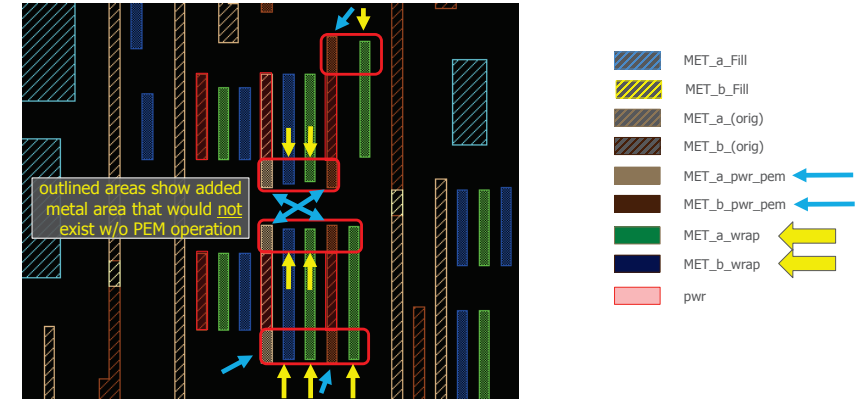
## FillPlus Code: Wrap Example On Colored Layers



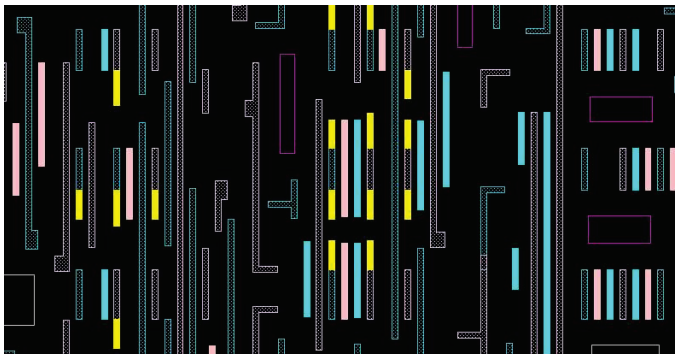




## FillPlus Code: Wrap Example On Colored Layers



## FillPlus (PEM+WRAP)+Design+POR SF (colored lyr)



Yellow: PEM extensions

Blue: MET_a wrap float

pink: MET_b wrap float

POR SF

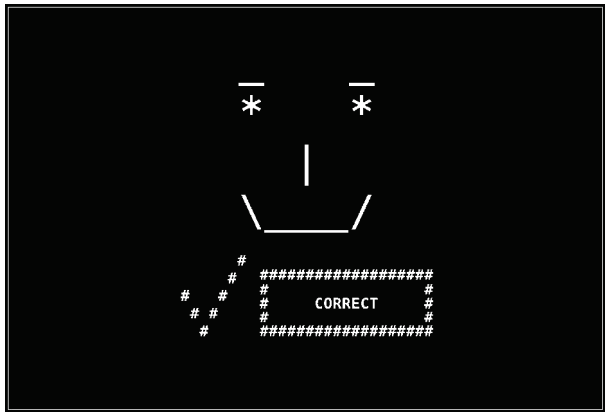
Design c1 shapes

Design c2 shapes




## Density Checks Now Clean after SF + FillPlus run

no density violations







# Thank you

Follow us on:
For more information, visit us at:
www.qualcomm.com & www.qualcomm.com/blog



## Summary of Qualcomm / Mentor Project

- Tried Track-Fill but goal was to use the proven fill solution
  - SmartFill is POR and therefore used as the process is developed
  - Solution that minimizes Post Fill Physical Verification time
- Analysis capabilities enabled the correct implementation
  - Achieved density rules
  - Minimized timing impact
  - Fits in the design flow
  - Understand the DRC rules and produces DRC clean results
- Qualcomm stated that it was the only feasible solution
- More to design closure then just fill
  - How do you handle last minute ECO changes post fill?
  - What can be done to reduce IR and EM issues?

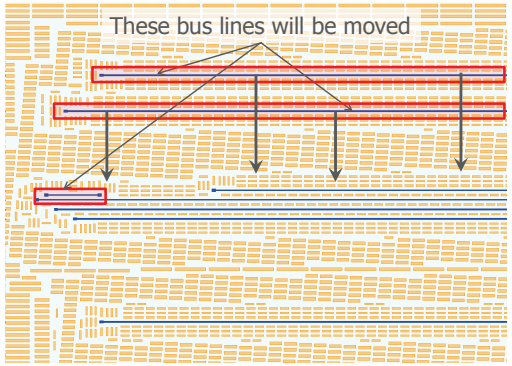
## Designed to Handle Last Minute Design Changes

- Benefits of ECO fill flow demonstrated on multiple designs
  - Reduced run time by only modifying fill in areas of ECO changes
  - Minimizes timing impact by only modifying fill around ECO changes
  - Minimizes mask cost because full refill alters fill on non-ECO layers
- Each point confirmed by results
  - Runtime reduction for ECO fill run time
  - Customer validated the timing impact was minimized
  - Reduction in mask cost was validated in the SPIE paper
- Push button solution that uses the POR fill deck





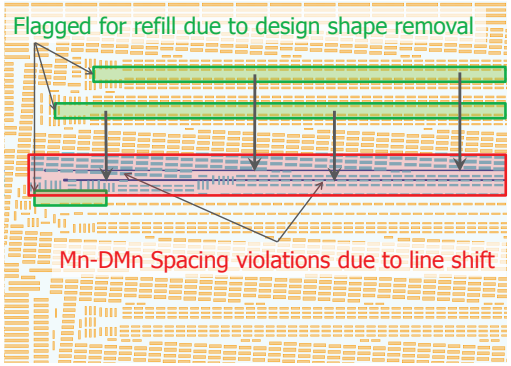
## M4 Ref_db Design with Original Fill







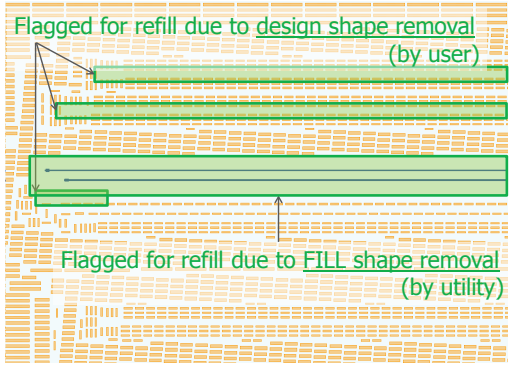
## M4 Original Fill with ECO changes



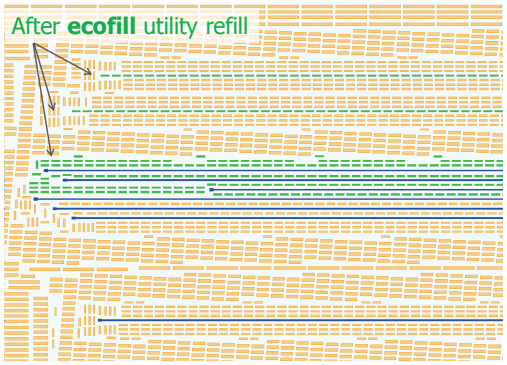




## M4 areas to refill



## M4 shapes added during refill stage

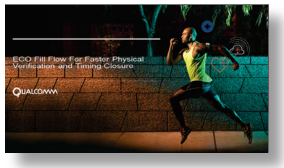




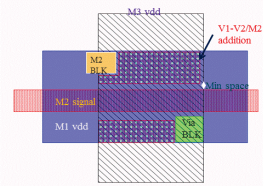



## Design Flows Success at Qualcomm

- ECO Fill Flow
  - Goal is to reduce time to market by automating the fill flow after ECO changes are made
  - Qualcomm presented at a previous DAC
    - Validate no timing impact
    - Fill run time improvement 12X with no manual cleanup




- PowerVia flow
  - Goal is to reduce IR or EM issues by properly inserting additional vias
  - Push button flow that takes care of the complex via rules
  - Number of designs have successfully used this flow
    - Used in either a P&R block or at the IP level



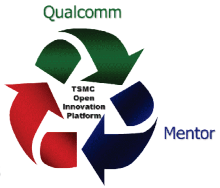





## Summary of the Fill Ecosystem

- Layout modification is enabled with advanced SVRF commands
  - Makes it easier to create and maintain layout enhancing decks
    - Allows users to extend fill decks if required
  - YieldEnhancer provides multiple algorithms so design teams can meet the challenges of achieving design closure

- Qualcomm is to leveraging a number of proven solution from Calibre
  - SmartFill is the POR fill solution at TSMC
  - ECO Fill Flow has been successfully used at multiple sites
    - Manages last minute design changes with a push of a button
  - Power Via Flow in use and helping to reduce reliability issues

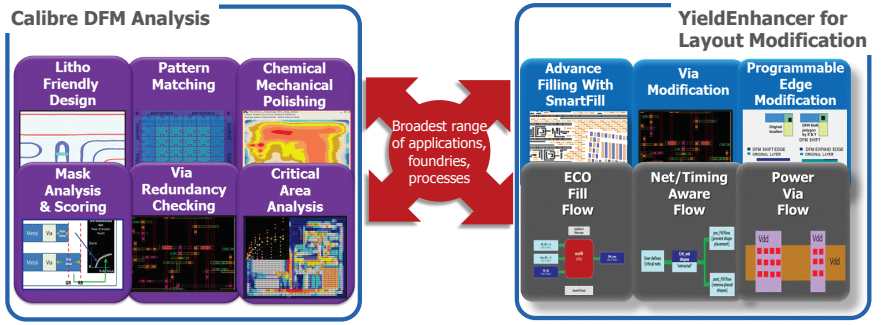







## Calibre World's Leading DFM Solutions

**Analysis and Layout Modification for Yield and Reliability Improvement**




Mentor®
A Siemens Business
www.mentor.com/perc